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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/995,594	11/29/2001	Takashi Yamada	216692US2	2712

22850 7590 09/02/2003

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EXAMINER
DICKEY, THOMAS L

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/995,594	YAMADA ET AL.	
	Examiner	Art Unit	
	Thomas L Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *16-28* is/are withdrawn from consideration.

5)☒ Claim(s) *7,8 and 14* is/are allowed.

6)☒ Claim(s) *1-6,9-13,15 and 29* is/are rejected.

7)☒ Claim(s) *30 and 31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The amendment filed on 07/07/03 has been entered.

Claim Objections

2. Applicant is advised that should claim 5 be found allowable, claim 9 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

A. Claims 5 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by DAVARI ET AL. (6,333,532).

Davari et al. discloses a semiconductor chip with a base substrate 12, a bulk device region (Memory) having a bulk growth layer on a part of the base substrate 12, the bulk device region (Memory) having a first device-fabrication surface in which a bulk device 30 is positioned on the bulk growth layer, an SOI device region (Logic) having a buried insulator 17 on the other part of the base substrate 12 and an SOI layer 18 on the buried insulator 17, the SOI device region (Logic) having a second device-fabrication surface in which an SOI device 28 is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level, and a boundary layer located at the boundary between the bulk device region (Memory) and the SOI device 28 region (Logic), further comprising a p-n junction (the edge of source 33) formed in the bulk device region (Memory) and positioned above the an interface between the base substrate 12 and the bulk growth layer. Note figure 2b of Davari et al.

A. Claims 1,2, and 10-13 stand rejected under 35 U.S.C. 102(a) as being anticipated by LEOBANDUNG et al. (6,180,486).

With regard to claims 1 and 2, Leobandung et al. discloses a semiconductor chip a base substrate 10; a bulk device region 38 having a bulk growth layer 34 on a part of the base substrate 10, the bulk device region 38 having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer 34; an SOI device region 40 having a buried insulator 12 on the other part of the base substrate 10 and an SOI

layer 14 on the buried insulator 12, the SOI device region 40 having a second device-fabrication surface in which an SOI device is positioned on the SOI layer 14, the first and second device-fabrication surface being positioned at a substantially uniform level; and a boundary layer, being the portion of bulk layer 34 that is located on the boundary, located at the boundary between the bulk device region 38 and the SOI device region 40, and further comprising a first isolation 28 in the bulk device region 38, a second isolation 30 in the SOI device region 40, wherein the bulk growth layer 34 is a silicon bulk growth layer, and the boundary layer reaches the base substrate 10 and is made of one of polysilicon or silicon-based compound semiconductors. Note figures 7 and 8 and column 3 lines 37-38 and column 5 lines 12-67 of Leobandung et al.

With further regard to claim13, Leobandung et al. further discloses a dummy pattern (no part #, it is seen on the right side of figure 7, mirroring part 28) in the bulk device region 38 near the boundary. Note figure 7 of Leobandung et al.

With regard to claim 10, Leobandung et al. discloses a semiconductor chip comprising a base substrate 10; a bulk device region 38 having a bulk growth layer 34 on a part of the base substrate 10, the bulk device region 38 having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer 34; an SOI device region 40 having a buried insulator 12 on the other part of the base substrate 10 and an SOI layer 14 on the buried insulator 12, the SOI device region 40 having a second device-fabrication surface in which an SOI device is positioned on the SOI layer 14, the first and second device-fabrication surface being positioned at a

substantially uniform level; and a boundary layer located at the boundary between the bulk device region 38 and the SOI device region 40, further comprising a first isolation 28 in the bulk device region 38, a second isolation 30 in the SOI device region 40, and a third isolation 32 positioned at the boundary and functioning as the boundary layer, the second isolation 30 being shallower than the third isolation 32. Note figures 7 and 8 and column 3 lines 37-38 and column 5 lines 12-67 of Leobandung et al.

With regard to claims 11 and 12, Leobandung et al. discloses a semiconductor chip comprising a base substrate 10; a bulk device region 38 having a bulk growth layer 34 on a part of the base substrate 10, the bulk device region 38 having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer 34; an SOI device region 40 having a buried insulator 12 on the other part of the base substrate 10 and an SOI layer 14 on the buried insulator 12, the SOI device region 40 having a second device-fabrication surface in which an SOI device is positioned on the SOI layer 14, the first and second device-fabrication surface being positioned at a substantially uniform level; and a boundary layer located at the boundary between the bulk device region 38 and the SOI device region 40, and further comprising a first isolation 28 in the bulk device region 38, and a second isolation 32 that is shallower than the first isolation 28, the boundary layer being the second isolation 32 because the second isolation 32 is positioned closest to the boundary, wherein the second isolation 32 functions as the boundary layer, and has a bottom face that is in contact with the

"buried oxide" 12. Note figures 7 and 8 and column 3 lines 37-38 and column 5 lines 12-67 of Leobandung et al.

B. Claims 1,3,4, and 6 stand rejected under 35 U.S.C. 102(a) as being anticipated by CHEN et al. (6,214,653).

With regard to claims 1,3, and 4, Chen et al. discloses a semiconductor chip with a base substrate 101; a bulk device region (labeled "High power circuits for CMOS DRAM/BULK") having a bulk growth layer on a part of the base substrate 101, the bulk device region having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer; an SOI device region (labeled "logic, high speed circuits for CMOS/SOI) having a buried insulator 102 on the other part of the base substrate 101 and an SOI layer (marked "Si") on the buried insulator 102, the SOI device region having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level; and a boundary layer 104 (left most instance) located at the boundary between the bulk device region and the SOI device region, wherein the bulk device region includes a first isolation 104 (left most instance) separating the bulk device, and the SOI device region includes a second isolation 104 (middle instance) separating the SOI device, the first and second isolations being of substantially the same depth and the first and second isolations have a depth reaching the buried insulator 102. Note figure 1D of Chen et al.

With regard to claim 6, Chen et al. discloses a semiconductor chip with a base substrate 101; a bulk device region (labeled "High power circuits for CMOS DRAM/BULK") having a bulk growth layer on a part of the base substrate 101, the bulk device region having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer; an SOI device region (labeled "logic, high speed circuits for CMOS/SOI) having a buried insulator 102 on the other part of the base substrate 101 and an SOI layer (marked "Si") on the buried insulator 102, the SOI device region having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level; and a boundary layer 104 (left most instance) located at the boundary between the bulk device region and the SOI device region, further comprising a first isolation 104 (right most instance) in the bulk device region, a second isolation 104 (middle instance) in the SOI device region, and a third isolation 104 (left most instance) positioned at the boundary arid functioning as the boundary layer, the first, second, and third isolations being of substantially the same depth. Note figure 1D of Chen et al.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 1 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over DAVARI ET AL. (6,333,532) in view of ADKISSON ET AL. (6,350,653).

Davari et al. discloses a semiconductor chip with a base substrate 12, a bulk device region (Memory) having a bulk growth layer on a part of the base substrate 12, the bulk device region (Memory) having a first device-fabrication surface in which a bulk device 30-35 is positioned on the bulk growth layer, an SOI device region (Logic) having a buried insulator 17 on the other part of the base substrate 12 and an SOI layer 18 on the buried insulator 17, the SOI device region (Logic) having a second device-fabrication surface in which an SOI device 28 is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level, and a boundary layer located at the boundary between the bulk device region (Memory) and the SOI device 28 region (Logic). Davari et al. further discloses that the bulk device 30-35 positioned in the bulk device region (Memory) includes a DRAM cell 30-35 having a trench capacitor 35 and a MOSFET 30, wherein the MOSFET 30 is positioned between the trench capacitor 35 and the boundary layer. Note figure 2b of Davari et al.

Davari et al. does not disclose a first isolation formed in a bulk device region so as to separate the bulk device, and a second isolation formed in the SOI device region so as to separate the SOI device.

However, Adkisson et al. discloses a semiconductor chip with a first isolation 54 formed in a bulk device region over a base substrate so as to separate the bulk device,

and a second isolation 80 formed in a SOI device region so as to separate the SOI device. Note figures 5 and 8 of Adkisson et al. Adkisson et al. informs the reader that first isolation 54 is necessary to separate multiple memory cells from each other in the bulk region, and that second isolation 80 is necessary to separate multiple logic elements from each other in the SOI region. Therefore, it would have been obvious to a person having skill in the art to replace augment Davari et al.'s semiconductor chip with the first and second isolations such as taught by Adkisson et al. in order to separate multiple memory cells and separate multiple logic elements to thus provide multiple memory cells and multiple logic elements on a single semiconductor chip, thus increasing functionality and decreasing costs.

B. Claim 15 stands rejected under 35 U.S.C. 103(a) as being unpatentable over LEOBANDUNG ET AL. (6,180,486) in view of SATO et al., 2000 symposium on VLSI Technology Digest, pages 82-83 (13 June 2000).

Leobandung et al. discloses a semiconductor chip with all the limitations of claim 15 except a DRAM cell in the bulk region having a trench capacitor, the trench capacitor comprising a first part extending at and below the interface between the base substrate and the bulk growth layer, and a second part extending above the interface, the width of the first part being greater than that of the second part. Note figures 7 and 8 and column 3 lines 37-38 and column 5 lines 12-67 of Leobandung et al.

However, Sato et al. discloses a DRAM cell in a bulk region having a trench capacitor (identified as the combination of the "storage node" and the "storage node

plug"), the trench capacitor comprising a first part ("storage node") extending at and below the interface between the base substrate and the bulk growth layer, and a second part ("storage node plug") extending above the interface, the width of the first part being greater than that of the second part. Note figure 2 of Sato et al. Therefore, it would have been obvious to a person having skill in the art to augment Leobandung et al.'s semiconductor chip with the DRAM cell in a bulk region having a trench capacitor, the trench capacitor comprising a first part extending at and below the interface between the base substrate and the bulk growth layer, and a second part extending above the interface, the width of the first part being greater than that of the second part, such as taught by Sato et al. in order to compactly combine logic circuits and memory circuits on a single chip.

Allowable Subject Matter

5. The following are indications of allowability:

A. Claims 7,8 and 14 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a semiconductor chip comprising a base substrate, a bulk device region having a bulk growth layer on a part of the base substrate, the bulk device region having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer, an SOI device region having a buried insulator on the other part of the base substrate and an SOI layer on the buried insulator, the SOI device region having a second device-

fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level, and a boundary layer located at the boundary between the bulk device region and the SOI device region, further comprising a first isolation in the bulk device region, a second isolation in the SOI device region, and a third isolation positioned at the boundary and functioning as the boundary layer, the first, second, and third isolations being of substantially the same depth, the first, second, and third isolations being deeper than the buried insulator, as recited in claim 7, or further comprising a dummy pattern in the bulk device region near the boundary, the dummy pattern is being a dummy capacitor, wherein the bulk device includes a DRAM cell having a trench capacitor, as recited in claim 14.

B. Claims 30 and 31 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments filed 07/07/03 have been fully considered but they are not persuasive.

It is argued, at page 11 of the remarks, that "Claim 1 has been amended to recite the first and second isolations formerly recited in claim 3, thus no new matter has been

added." For the record, the examiner responds that this is not quite true, that claim 1 has in fact been amended to recite a broad version of the first and second isolations formerly recited in any of dependent claims 3,4,6,10,11, and 12, thus no new matter has been added to the recitals of claims 1,3,4,6,10,11, and 12. Claims 2,5,9 (claim 9 being a word for word duplicate of claim 5), 13, and 15, recite combinations not previously recited in the claims, for which support can be found in the original specification at figures 2 and 10.

It is argued, at page 10 of the remarks, that "[Claim 5 was] objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form." For the record, the examiner responds that this is not quite true. In fact claim 5 was objected to as being dependent upon a rejected base claim, but would have been allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. It is noted that claim 5, as rewritten, does not include all of the limitations of base claim 1 and intervening claims 3 and 4, noting that claim 5, before being rewritten, recited dependence on claim 4.

It is argued, at page 12 of the remarks, that "Leobandung et al. fails to show claimed first and second isolations." However, part 28 in figure 7 is an isolation region forming a contiguous part of bulk region 38, and part 30 in figure 7 is an isolation region forming a contiguous part of SOI region 40.

It is argued, at page 12 of the remarks, that "Fig. 8 of Leobandung et al. shows a planar SOI structure having an oxide region 36..." However, this is irrelevant. Oxide

region 36 is not part of the claimed invention as disclosed by Leobandung et al., and the examiner has never maintained that it was.

It is argued, at page 12 of the remarks, that "[t]rench bottom oxide layer 28 in fig. 7 of Leobandung et al. is etched to form a smaller trench which is then filled with an oxide." However, it is noted that the features upon which applicant relies (i.e., that the invention cannot have a smaller trench in the bottom oxide SOI layer which is then filled with an oxide.) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

It is argued, at page 12 of the remarks, that "Leobandung et al. are silent claimed dummy pattern in the device region near the boundary." However, it is axiomatic that the reference describing the prior art device need not identify an element using the same words the claimant uses. The part seen mirroring part 28 in figure 7 of Leobandung et al. is a patterned part, it is in the device region near the boundary, and it is a dummy part insofar as it serves no purpose otherwise required of the claimed invention.

It is argued, at page 12 of the remarks, that "Chen et al. fails to show the claimed first isolation." However, all that is required of the claimed first isolation is that it be an isolation formed in the bulk device region so as to separate the bulk device region. The left most part labeled "104" is formed in the bulk device region (on the boundary

between the bulk device region and the SOI region), and it serves both to isolate, and to separate the bulk device region.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on Tues-Friday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers

for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 306-3431.

tld
08/2003

Minhloan Tran
Primary Examiner
Art Unit 2826